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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

in re application of: Chung-Hui Chen Examiner: Unknown

Serial No.: 10/791,044 Group Art Unit: Unknown

Filed: March 1, 2004 Attorney Docket No.: N1280-00070(TSMC2003-0817)

For: IMPROVED DOUBLE-EDGE-TRIGGER FLIP-FLOP

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

This Information Disclosure Statement is being filed in connection with the patent application referenced above. The Examiner is requested to consider each of the references cited herein and forward an initialed copy of the enclosed PTO Form 1449 to the undersigned representative. This Statement is being filed:

	3	Upon f	iling the application.						
continue			three months from the filing date of this application, which is not a application.						
]	Within	thin three months from date of entry of the national stage for this application.						
]	Before	e the mailing date of a first Office action on the merits for this application.						
Continued			efore the mailing date of a first Office action after the filing of a request for nation.						
Allowand is accomp	ce, and	d (iii) a	the mailing date of any of: (i) a Final Office Action, (ii) a Notice of any other action that closes prosecution of this application. The Statement						
			A Statement pursuant to 37 C.F.R. §1.97(e) or						
		The fee set forth in 37 C.F.R. §1.17(p), believed to be							
			Before payment of the Issue Fee. The Statement is accompanied by:						
			A Statement pursuant to 37 C.F.R. §1.97(e) and						
			The fee set forth in 37 C.F.R. §1.17(p), believed to be						

I.	Provision of Copies
enclos	A copy of each of the references listed on the attached Form PTO Form 1449 is herewith and forms a part hereof.
part he	A translation of References AA, AB and AC are enclosed herewith and form a of.
applica	A copy of the European Search Report from a corresponding or related EPO on is enclosed herewith.
applica	A copy of the International Search Report from a corresponding or related PCT on is enclosed herewith.
	This application claims priority, pursuant to 35 U.S.C. §120, to prior U.S. ion No, filed References not submitted herewith were d to or cited by the Office in the prior application(s).
II.	'ee
	No fee is believed due in connection with filing of this Statement. However, in a fee or refund is due, the Commissioner is authorized to charge any fee associated communication or credit any overpayment to Deposit Account No. 04-1679 (N1280-
	The fee in the amount \$ that is due in connection of filing of this nt was paid upon electronic filing of a corresponding Statement, which was made on using the ePAVE software.
to be d	The fee set forth in 37 C.F.R. §1.17(p), believed to be \$, is believed in connection of filing of this Statement.

A check in the amount \$_____ is enclosed.

Respectfully submitted,

The Commissioner is authorized to charge any other fee associated with this

Dated: 4/26/04

Howard Chen, Reg. No. 44,615

Attorney For Applicant

DUANE MORRIS LLP

One Market Street, Spear Tower, Suite 2000

San Francisco, CA 94105-1104

(415) 371-2200 (Telephone)

(415) 371-2201 (Fax)

communication, or credit any overpayment, to Deposit Account No. 04-1679 (N1280-00070).

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Form PTO-	1449 Mo	dified	Docket No. N1280-00070(TSMC2003-817)		Serial No. 10/791,044			
List of Pate Cited by Ap (Use severa	pplicant		Applicant Chung-Hui Chen					
U.S. Depart Patent and			Filing Date 03/1/2004		Group Unknown			
U. S. PATE	NT DOC	UMENTS						
Examiner [;] Initial	Cite No.	Document No.	Kind Code (if known)	Name	Date	Class	Subclass	
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initial	Cite No.	(Include name of author in CAPITAL LETTERS, Title of the Article (when appropriate) title of the item (book, magazine, journal, symposium, catalog, etc.) date, pages, volume, issue number(s), publisher, city and/or country where published)	Т
	5.	Ker, Ming-Dou et al., "CAPACITOR-COUPLE ESD PROTECTION CIRCUIT FOR DEEP-SUBMICRON LOW-VOLTAGE CMOS ASIC", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 4, No. 3, (SEPT. 1996), pp. 307-321	
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	7.	Wu et al., A NEW ON-CHIP ESD PROTECTION CIRCUIT WITH DUAL PARASITIC SCR STRUCTURES FOR CMOS VLSI, IEEE Journal of Solid-State Circuits, Vol. 27, No. 3, (MAR 1992), pp. 274-280	

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.